



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,077	06/28/2001	Dean Alan Kalman	RPS920000119US1	6529

28722 7590 05/03/2004

BRACEWELL & PATTERSON, L.L.P.  
P.O. BOX 969  
AUSTIN, TX 78767-0969

EXAMINER

LOHN, JOSHUA A

ART UNIT	PAPER NUMBER
----------	--------------

2114

13

DATE MAILED: 05/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/894,077

Applicant(s)

KALMAN, DEAN ALAN

Examiner

Joshua A Lohn

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 April 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>  </u> | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 10, 11, 13-19, and 22-<sup>24</sup>~~25~~ are rejected under 35 U.S.C. 102(b) as being anticipated by Kakuta et al., United States Patent number 5,600,783, published February 4, 1997.

As per claim 1, Kakuta discloses a method of servicing a request to a redundant storage array including a plurality of storage media containing data and related parity data, see column 3, lines 10-32. Kakuta further discloses receiving a data request for data stored by a selected storage medium among the plurality of storage media and in response to receiving the data request while an update to the selected medium is being performed (medium is withdrawn from operation), servicing the data request by reference to the data and the related parity data of other storage media among the plurality of storage media, see column 9, lines 43-53.

As per claim 2, Kakuta discloses automatically reconstructing requested data utilizing the data and related parity data from the other storage media and outputting the reconstructed requested data, see column 9, lines 38-42.

As per claim 3, Kakuta discloses determining a type of the data request, see column 9, lines 5 and 54. Kakuta also discloses automatically reconstructing requested data utilizing the data and the related parity data only in response to determining that the data request is a data read request, see column 9, lines 38-42.

Art Unit: 2114

As per claim 4, Kakuta discloses in response to determining that the data request is a data write request, logging the data write request and storing new data for the data write request, see column 10, lines 45-53. Kakuta also discloses setting the particular storage medium to a rebuild status, indicated by the board withdrawal flag that indicates a need to rebuild a disk and rebuilding the particular storage medium utilizing the data and related parity data from the other storage media, see column 10, line 45 through column 11, line 16. Kakuta also discloses setting the particular storage medium to online status, see column 1, lines 22-34.

As per claim 5, Kakuta discloses receiving a data request for data stored by a particular storage medium comprises receiving a data request for data stored by a particular disk of the redundant disk array, see column 9, lines 5-7 and 54-56.

As per claim 6, Kakuta discloses an adapter for use with a data processing system including a redundant storage array including a plurality of storage media containing data and related parity data, see column 3, lines 10-32. Kakuta also discloses an updating circuit for receiving a data request for data stored by a selected storage medium among the plurality of storage media and a request servicing circuit, in response to receiving the data request while an update to the selected storage medium is being performed (medium is withdrawn from operation), for servicing the data request by reference to the data and the related parity data of other storage media among the plurality of storage media, see column 9, lines 43-53.

As per claim 7, Kakuta disclose the updating circuit being an adapter processor, see the array controller, element 2 of figures 1 and 3, which acts as an adapter processor and includes all updating circuitry.

Art Unit: 2114

As per claim 10, Kakuta discloses a storage location for temporarily storing write data for the selected storage media during the updating, see column 10, lines 45-53.

As per claim 11, Kakuta discloses the storage location is an adapter cache, see column 10, lines 51-53.

As per claim 13, Kakuta discloses the data request is a data read request, see column 9, line 5.

As per claim 14, Kakuta discloses a disk drive system comprising an adapter according to claim 6 above, where the adapter is element 2 of figures 1 and 3. This adapter satisfies all the limitations of claim 6 as is described in the above rejection. Kakuta also discloses a redundant storage array, see column 3, lines 10-32.

As per claim 15, Kakuta discloses the redundant storage array is a redundant array of inexpensive disks (RAID), see column 6, lines 17-18.

As per claim 16, Kakuta discloses a data processing system comprising a system processor, CPU of figure 1. It is inherent that a system memory is coupled to the system processor. This is inherent because some form of system memory must exist to receive and store during execution all the data requested by and sent from the system processor, see column 9, lines 5-7 and 54-56. Kakuta also discloses a redundant storage array, see column 3, lines 10-32. Kakuta discloses an adapter including a redundant storage array including a plurality of storage media containing data and related parity data, with the adapter including an updating circuit for

Art Unit: 2114

receiving a data request for data stored by a selected storage medium among the plurality of storage media and a request servicing circuit, in response to receiving the data request while an update to the selected storage medium is being performed (medium is removed from operation), for servicing the data request by reference to the data and the related parity data of other storage media among the plurality of storage media, see column 9, lines 43-53.

As per claim 17, Kakuta discloses the redundant storage array is a redundant array of inexpensive disks (RAID), see column 6, lines 17-18.

As per claim 18, Kakuta discloses the redundant storage array stores data in stripes, wherein each stripe further includes data and related parity data, see column 5, lines 23-28, where the stripe is represented in a logical group.

As per claim 19, Kakuta discloses the updating circuit is an adapter processor, see the array controller, element 2 of figures 1 and 3, which acts as an adapter processor and includes all updating circuitry.

As per claim 22, Kakuta discloses a storage location for temporarily storing all write data for the selected storage media during the updating, see column 10, lines 45-53.

As per claim 23, Kakuta discloses the storage location is a temporary space on other storage media of the redundant storage array, see column 14, lines 18-20, and column 13, lines 40-50.

As per claim 24, Kakuta discloses the storage location is an adapter cache, see column 10, lines 51-53.

Art Unit: 2114

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 8, 9, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakuta, in view of Lubbers et al., United States Patent number 5,774,643, published June 30, 1998.

As per claim 8, Kakuta discloses all the limitations relating to the dependency from claim 6, however Kakuta fails to disclose the request servicing circuit is an exclusive-OR (XOR) processor for automatically reconstructing requested data utilizing data and related parity data from other storage media during the updating, in response to a data request by the system processor, the XOR processor coupled to an adapter processor.

Lubbers discloses an XOR processor for reconstructing requested data using data and related parity from other storage media, with this XOR processor being connected to the drive array controller that acts as an adapter processor, see column 4, lines 9-25.

It would have been obvious to one skilled in the art at the time the invention was made to include the XOR processor of Lubbers in the parity device provided for by Kakuta.

This would have been obvious because Kakuta discloses a parity device that is used to reconstruct data utilizing the data and related parity data from other storage device, see column 9, lines 38-42. Kakuta discloses this parity device acting as a data recovery circuit that is part of

Art Unit: 2114

an adapter processor, see figure 3, element 18. Kakuta fails to describe the interior workings of the parity generator. Lubbers discloses a method that provides the detailed workings of a parity generator. These workings include the XOR processor described above as an often used convenient way of determining parity information, see column 3, lines 65-67. It would have been obvious to include this functionality in the parity generator of Kakuta because of the convenience and ability to reconstruct data as is desired by Kakuta.

As per claim 9, Kakuta discloses all the limitations relating to the dependency form claim 6, however Kakuta fails to disclose a non-volatile random access memory (NVRAM) for logging data write requests.

Lubbers discloses using a non-volatile random access memory for logging data write requests, see column 4, lines 50-52.

It would have been obvious to one skilled in the art at the time of the invention to include the non-volatile random access memory of Lubbers in the invention of Kakuta.

This would have been obvious because Kakuta discloses using the memory of the disk array controller cache to store all write operations, see column 10, lines 50-53. It would have been obvious to one skilled in the art at the time of the invention to include a non-volatile cache memory to have the added benefit of tolerance of any data errors caused by system crashes, as described by Lubbers, see column 4, lines 50-67.

As per claim 20, the data processing system according to claim 18 is described in the rejection of claim 18 provided above in reference to the teachings of Kakuta. The additional



Art Unit: 2114

limitation of the XOR processor is taught in the disclosure of Lubbers and reasonable motivation exists to combine the two teachings is provided in the above rejection of claim 8. The same motivation exists for claim 20 as that used in the rejection of claim 8 and is omitted for purposes of brevity, as the rejection of claim 20 is identical to that provided for claim 8.

As per claim 21, the data processing system according to claim 16 is described in the rejection of claim 16 provide above in reference to the teachings of Kakuta. The additional limitation of a non-volatile random access memory (NVRAM) for logging all data write requests and data read-with-intent-to-write requests is taught in the disclosure of Lubbers, which logs all requests involving write operations, see column 4, lines 50-67, and would include writes and read-with-intent-to-write requests as they are included together in the disclosure of Lubbers, see column 9, lines 42-55.

It would have been obvious to one skilled in the art at the time of the invention to include the non-volatile random access memory of Lubbers in the invention of Kakuta.

This would have been obvious because Kakuta discloses using the memory of the disk array controller cache to store all write operations, see column 10, lines 50-53. It would have been obvious to one skilled in the art at the time of the invention to include a non-volatile cache memory to have the added benefit of tolerance of any data errors caused by system crashes, as described by Lubbers, see column 4, lines 50-67.

Claims 12 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakuta, in view of Surugucchi et al., United States Patent number 6,098,119, published August 1, 2000.

Art Unit: 2114

As per claim 12, Kakuta discloses all the limitations relating to the dependency form claim 11, however Kakuta fails to disclose the adapter cache further including a battery-backup circuit for preserving data stored on the adapter cache.

Suruguchi discloses an adapter cache using a battery backup, see column 6, lines 30-34.

It would have been obvious to one skilled in the art at the time of the invention to use the adapter cache of Suruguchi in the adapter of Kakuta.

This would have been obvious because Kakuta and Suruguchi both disclose a cache implemented in an adapter that functions as a RAID controller, see figure 3 of Kakuta and column 6, lines 22-24 of Suruguchi. Since both systems use a similar cache it would have been obvious to include the battery backup, taught by Suruguchi, to provide the obvious benefit of tolerance of a system crash or power failure, see column 6, lines 32-34 of Suruguchi.

As per claim 25, the data processing system according to claim 24 is described in the rejection of claim 24 provided above in reference to the teachings of Kakuta. The additional limitation of the adapter further including a battery backup circuit and the reasonable motivation existing to combine the two teachings is provided in the above rejection of claim 12. The same motivation exists for claim 25 as that used in the rejection of claim 12 and is omitted for purposes of brevity, as the rejection of claim 25 is identical to that provided for claim 12.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kakuta, in view of Ritchie, United States Patent 4,135,240, published January 16, 1979.

Art Unit: 2114

Kakuta discloses receiving a data request for data stored by a selected storage medium among a plurality of storage media and in response to receiving the data request while an update to the selected storage medium is being performed (medium is withdrawn from operation), for servicing the data request by reference to data and related parity data of other storage media among the plurality of storage media, see column 9, lines 43-53.

Kakuta fails to disclose the above operations being performed using code from within a computer-readable medium.

Ritchie discloses implementing a design in a computer program.

It would have been obvious to one skilled in the art at the time the invention was made that the functionality of Kakuta could have been implemented in a software form.

This would have been obvious because Ritchie states in column 5, lines 48-53: "To those skilled in the computer art it is obvious that such an implementation can be expressed either in terms of a computer program (software) implementation or a computer circuitry (hardware) implementation, the two being functional equivalents of one another". Thus it would have been obvious to implement the device of Kakuta in a software form to gain the benefits of software without sacrificing any functionality of hardware.

Art Unit: 2114

*Conclusion*


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is provided on from PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A Lohn whose telephone number is (703) 305-3188. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoleil can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL



**SCOTT BADERMAN**  
**PRIMARY EXAMINER**